=> d his

(FILE 'HOME' ENTERED AT 08:50:24 ON 01 OCT 2003)
FILE 'CA' ENTERED AT 08:50:34 ON 01 OCT 2003
L1 211109 S MASS(1A)(SPECTRO? OR SPECTRAL?)
L2 4504 S L1 AND(ETCH? OR SEMICONDUCT?)
L3 2851 S ENDPOINT(5A)(DETECT? OR DETERMIN? OR MONITOR? OR ESTIMAT? OR EVALUAT? OR ASSAY? OR ANALY? OR ASSES? OR EXAMIN? OR CHECK? OR SENSE# OR SENSING OR SENSOR OR IDENTIF?)
L4 4046 S CONTROL?(4A)ETCH?
L5 435 S (IMPLANT? OR DOPANT OR DOPED OR DOPING) AND L3-4
L6 8 S L2 AND L5
L7 221 S L5 AND SEMICONDUCT?
L8 22 S (ENDING OR STOPPING)(2A)POINT(5A)(DETECT? OR DETERMIN? OR MONITOR? OR ESTIMAT? OR EVALUAT? OR ASSAY? OR ANALY? OR ASSES? OR EXAMIN? OR CHECK? OR SENSE# OR SENSING OR SENSOR OR IDENTIF?)
L9 1 S L8 AND SEMICONDUCT?
L10 2 S L8 AND ETCH?
L11 9 S L3/TI,IT,ST AND L7
L12 212 S L7 NOT L11
L13 6 S L12 AND(ENDPOINT OR(ENDING OR STOPPING)(2A)POINT)
L14 36 S L8,L9-11,L13

=> d bib,ab 1-36

L14 ANSWER 1 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 139:158544 CA
TI Focused ion beam visual **endpoint detection** for etching of integrated circuits
IN Suthar, Sailesh C.; Hack, Paul J.; Sarwar, Syed Nabeel; Martinez, Mary J.
PA USA
SO U.S. Pat. Appl. Publ., 7 pp.
PI US 2003153192 A1 20030814 US 2002-76130 20020213
PRAI US 2002-76130 20020213
AB The application relates, generally, to integrated circuit processing and, more particularly, to **endpoint detection** for ion beam etching. The method comprises etching a backside of the **semiconductor** chip, the front side including a 1st well with a 1st type of **doping** and a 2nd well with a 2nd type of **doping**; monitoring a backside of the **semiconductor** chip during etching; and detg. when a 1st portion of the backside over 1 of the 1st and 2nd wells differs from a 2nd portion of the backside over the other of the 1st and 2nd wells. A method for etch **endpoint detection** includes etching a backside of a **semiconductor** chip, the **semiconductor** chip having ≥1 **doped** well formed proximate a front side of the **semiconductor** chip; monitoring the backside of the **semiconductor** chip during etching until ≥1 **doped** well becomes visible; and stopping etching after the **doped** well becoming visible.

L14 ANSWER 3 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 138:48354 CA
TI Method for vapor phase etching of silicon **semiconductors** in a low-pressure chamber
IN Patel, Satyadev R.; Schaadt, Gregory P.; MacDonald, Douglas B.; Shi, Hongqin; Huibers, Andrew G.; Heureux, Peter
PA Reflectivity, Inc., USA
SO U.S. Pat. Appl. Publ., 26 pp., Cont.-in-part of U.S. Ser. No. 954,864.
PI US 2002195423 A1 20021226 US 2002-104109 20020322
US 6290864 B1 20010918 US 1999-427841 19991026
US 2002121502 A1 20020905 US 2001-954864 20010917

PRAI US 1999-427841 A2 19991026
AB The etching of a material in a vapor phase etchant is disclosed where a vapor phase etchant is provided to an etching chamber at a total gas pressure of 10 torr or more, preferably 20 torr or even 200 torr or more and where the etching can be done with high selectivity with a good **detn**. of the **endpoint**. The vapor phase etchant can be gaseous acid etchant, a noble gas halide or an interhalogen. The sample/workpiece that is etched can be, for example, a **semiconductor** device or MEMS device, etc. The material that is etched/removed by the vapor phase etchant is preferably Si and the vapor phase etchant is preferably provided along with one or more diluents. Another feature of the etching system includes the ability to accurately det. the end point of the etch step, such as by creating an impedance at the exit of the etching chamber (or downstream thereof) so that when the vapor phase etchant passes from the etching chamber, a gaseous product of the etching reaction was monitored, and the end point of the removal process can be detd. The vapor phase etching process can be flow through, a combination of flow through and pulse, or recirculated back to the etching chamber. A 1st plasma or wet chem. etch (or both) can be performed prior to the vapor phase etch.

L14 ANSWER 5 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 135:379732 CA
TI Method and apparatus for endpointing a chemical-mechanical planarization process
IN Agarwal, Vishnu K.
PA Micron Technology, Inc., USA
SO U.S., 16 pp.
PI US 6323046 B1 20011127 US 1998-139814 19980825
US 6517668 B2 20030211
US 6562182 B2 20030513
PRAI US 1998-139814 A3 19980825
AB A method and app. for endpointing a planarization process of a microelectronic substrate. In one embodiment, the app. may include a species analyzer that receives a slurry resulting from the planarization process and analyzes the slurry to det. the presence of an endpointing material **implanted** beneath the surface of the microelectronic substrate. The species analyzer may include a mass spectrometer or a spectrum analyzer. In another embodiment, the app. may include a radiation source that directs impinging radiation toward the microelectronic substrate, exciting atoms of the substrate, which in turn produce an emitted radiation. A radiation detector is positioned proximate to the substrate to receive the emitted radiation and **det**. the **endpoint** by **detg**. the intensity of the radiation emitted by the endpointing material. The endpointing material may be selected to be easily detected by the species detector or the radiation detector, and may further be selected to be easily distinguishable from a matrix material that comprises the bulk of the microelectronic substrate.

L14 ANSWER 6 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 135:130891 CA
TI Method and laminate for fabricating an integrated circuit
IN Gabriel, Calvin Todd; Zheng, Tammy D.; De Muizon, Emmanuel; Leard, Linda A.
PA Philips Semiconductors, Inc., USA; Koninklijke Philips Electronics N.V.
SO PCT Int. Appl., 45 pp.
PI WO 2001056080 A1 20010802 WO 2001-US2652 20010126
US 6541359 B1 20030401 US 2000-495415 20000131
PRAI US 2000-495415 A 20000131
AB A method and app. are provided for fabricating an integrated circuit on a laminate having a gate electrode layer over a SiO2 layer. **Detection** of the

gate etch **endpoint** signal is improved by maximizing the use of a faster etching **dopant** material (e.g., n-type **dopant**) and minimizing the use of a slower etching **dopant** material (e.g., p-type **dopant**) in the gate electrode layer. In one embodiment, a 1st portion of the gate electrode layer, substantially corresponding only to the location at which a gate is to be formed, is **doped** with the slower etching **dopant** material. The remaining portion of the gate electrode layer is **doped** with the faster etching **dopant** material; thus, more of the gate electrode layer is **doped** with the faster etching **dopant** material than with the slower etching **dopant** material. A gate mask is aligned over the gate electrode layer, and the unmasked portions of the gate electrode layer are removed using an etchant. The n-**doped** portions of gate electrode layer will etch away faster, and because the gate electrode layer is predominantly n-type, a strong and **detectable endpoint** signal will be induced when the etchant reaches the SiO2 layer.

L14 ANSWER 7 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 135:115614 CA
TI Method and apparatus for **detecting** an ion-**implanted** polishing **endpoint** layer within a **semiconductor** wafer
IN Miller, Gayle W.; Chisholm, Michael F.
PA Lsi Logic Corp., USA
SO U.S., 13 pp.
PI US 6268224 B1 20010731 US 1998-108091 19980630
PRAI US 1998-108091 19980630
AB A method of fabricating a **semiconductor** wafer having a polishing endpoint layer which is formed by **implanting** ions into the wafer includes the step of polishing the wafer to remove material from the wafer. The method also includes the step of detecting a 1st change in friction when material of the ion-**implanted** polishing endpoint layer begins to be removed during the polishing step. The method further includes the step of detecting a 2nd change in friction when material of the ion-**implanted** polishing endpoint layer ceases to be removed during the polishing step. Also, the method includes the step of terminating the polishing step in response to detection of the 2nd change in friction. An app. for polishing a **semiconductor** wafer down to an ion-**implanted** polishing endpoint layer in the wafer is also disclosed.

L14 ANSWER 8 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 133:201894 CA
TI **Endpoint detection** method and apparatus which utilize a chelating agent to **detect** a polishing **endpoint** in **semiconductor** device fabrication
IN Shelton, Gail D.; Miller, Gayle W.
PA Lsi Logic Corporation, USA
SO U.S., 12 pp.
PI US 6117779 A 20000912 US 1998-212503 19981215
US 6383332 B1 20020507 US 2000-583434 20000531
PRAI US 1998-212503 A3 19981215
AB A method of planarizing a **semiconductor** wafer having a polishing endpoint layer that includes a ligand is disclosed. One step of the method includes polishing a 1st side of the wafer to remove the ligand from the wafer. Another step of the method includes detg. that a chelating agent has bound the ligand due to the polishing step removing the ligand of the polishing endpoint layer. The method also includes the step of terminating the polishing step in response to detg. that the chelating agent has bound the ligand. A polishing system is also disclosed which **detects** a polishing **endpoint** based upon a chelating agent binding a ligand of a polishing endpoint layer of a **semiconductor** device.

L14 ANSWER 9 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 133:36734 CA
TI Method of **detecting** a polishing **endpoint** layer of a **semiconductor** wafer which includes a non-reactive reporting species
IN Miller, Gayle W.; Shelton, Gail D.; Chisholm, Brynne K.
PA LSI Logic Corp., USA
SO U.S., 13 pp.
PI US 6080670 A 20000627 US 1998-131921 19980810
PRAI US 1998-131921 19980810
AB A method of planarizing a **semiconductor** wafer having a polishing endpoint layer that includes a S-contg. reporting species includes the step of polishing a 1st side of the wafer to remove material from the wafer. The method also includes the step of detecting presence of the S-contg. reporting species in the material removed from the wafer. The method further includes the step of terminating the polishing step in response to detecting presence of the S-contg. reporting species. A shallow trench isolation process for fabricating a **semiconductor** wafer is also disclosed.

L14 ANSWER 10 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 133:25509 CA
TI Optical monitoring system for Group III-V **semiconductor** wafer processing
IN Ressl, Michael G.
PA Lucent Technologies, Inc., USA
SO U.S., 7 pp.
PI US 6075909 A 20000613 US 1998-105712 19980626
PRAI US 1998-105712 19980626
AB An optical monitoring system for Group III-V **semiconductor** wafer processing in integrated circuit fabrication utilizes an optical transmitter/receiver assembly formed in the wafer at an early stage in the fabrication process. The optical transmitter is then activated, and the optical output signal is monitored during subsequent processing steps, such as ion **implantation** and layer deposition to assess the quality of the process. In one embodiment, the **monitoring** system is useful as an **endpoint detection** process.

L14 ANSWER 11 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 132:355737 CA
TI **Endpoint detection** method and apparatus which utilize an endpoint polishing layer of catalyst material for planarizing a **semiconductor** wafer
IN Chisholm, Brynne K.; Miller, Gayle W.; Shelton, Gail D.
PA LSI Logic Corporation, USA
SO U.S., 11 pp.
PI US 6071818 A 20000606 US 1998-109331 19980630
US 6258205 B1 20010710 US 2000-534652 20000324
PRAI US 1998-109331 A3 19980630
AB A method of planarizing a **semiconductor** wafer having a polishing endpoint layer that includes a catalyst material is disclosed. One step of the method includes polishing a 1st side of the wafer to remove material from the wafer. Another step of the method includes detg. that a catalytic reaction occurred due to the polishing step removing the catalyst material of the polishing endpoint layer. The method also includes the step of terminating the polishing step in response to detg. that the catalytic reaction occurred. A polishing system is also disclosed which **detects** a polishing **endpoint** based upon a catalytic reaction triggered by a catalyst material of a polishing endpoint layer of a **semiconductor** device.

L14 ANSWER 14 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 131:109906 CA
TI Method of plasma etching **doped** polysilicon layers with uniform etch rates

IN Leverd, Francois; MacCagnan, Renzo; Mass, Eric
PA International Business Machines Corp., USA
SO Eur. Pat. Appl., 11 pp.
PI EP 932191 A1 19990728 EP 1997-480107 19971230
US 2001001729 A1 20010524 US 1998-213611 19981218
PRAI EP 1997-480107 A 19971230
AB In wafer **semiconductor** manuf., a method of etching an arsenic **doped** polysilicon layer down to a patterned borophosphosilicate glass (BPSG) layer provided with a plurality of openings with an uniform etch rate is disclosed. The method relies on a combination of both system and process improvements. The system improvement consists to hold the wafer in the reactor during the etch process with an electrostatic chuck device to have a perfect plasma environment around and above the wafer. On the other hand, the process improvement consists in the use of a non-**dopant** sensitive and not selective chem. A NF3/CHF3/N2 gas mixt. with a 11/8.6/80.4 ratio in percent is adequate in that respect. The etch time duration is very accurately **controlled** by an optical **etch endpoint detection** system adapted to **detect** the intensity signal transition of a CO line at the BPSG layer exposure. The process is continued by a slight overetching. When the above method is applied to the **doped** polysilicon strap formation in DRAM chips, excessive or insufficient etching of the polysilicon layer is avoided, so that the **doped** polysilicon strap thickness is thus much more uniform, opening to opening, within a wafer.

L14 ANSWER 15 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 129:116590 CA
TI Dynamic images of plasma processes: Use of Fourier blobs for **endpoint detection** during plasma etching of patterned wafers
AU Rietman, Edward A.; Lee, John Tseng-Chung; Layadi, Nace
CS Bell Labs, Lucent Technologies, Murray Hill, NJ, 07974, USA
SO Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films (1998), 16(3, Pt. 2), 1449-1453
AB By monitoring various process parameters (e.g., applied radiofrequency power, flow rate of gases, etc.) as a function of time, Fourier series decompn. of the values of those parameters, at each time step, plotted on polar coordinates, gives closed curves representing the state of the plasma and the activity on the wafer. A change of the shape of the blob is a signature of the endpoint. The technique was successfully applied on TiN/poly-Si, WSix, and **doped** poly-Si gate etch, and contact etch processes. Also, the method is reproducible from wafer to wafer and can be used easily by inexperienced operators to spot endpoint in plasma processes.

L14 ANSWER 20 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 121:46637 CA
TI Phase-shifting lithographic mask having phase-shifting layers of differing compositions
IN Pierrat, Christophe
PA American Telephone and Telegraph Co., USA
SO Eur. Pat. Appl., 7 pp.
PI EP 583942 A2 19940223 EP 1993-306358 19930811
US 5405721 A 19950411 US 1993-164735 19931208
PRAI US 1992-931621 19920818
AB A phase-shifting lithog. mask, for use in conjunction with optical radiation of wavelength λ, has a transparent substrate upon which are successively located a bottom $(2m + 1)\pi$ radian phase-shifting layer and a patterned top $(2n + 1)\pi$ radian phase-shifting layer, each having at least approx. the same refractive index at the wavelength λ as that of the substrate. A more finely patterned, opaque chromium layer is located on the patterned top

phase-shifting layer. The bottom phase-shifting layer is chem. different from both the substrate and the top layer, in order to provide either **etch-stopping** or end-**point etch detection** during subsequent dry ion beam millings, as with gallium ions, of either or both of the layers, for the purpose of mask repair. For example, the substrate is quartz, the bottom phase-shifting layer is calcium fluoride, and the top phase-shifting layer is silicon dioxide. Remnants of the gallium can be removed from both the exposed portions of the substrate and of the bottom layer, such as by forming indentation regions by means of successive **etchings**, for example, with HF and HCl, resp., for resp. prescribed time intervals having a ratio such that the relative phase shifts of the substrate and both phase-shifting layers are not disturbed by the resp. **etchings**.

L14 ANSWER 25 OF 36 CA COPYRIGHT 2003 ACS on STN
AN 107:125429 CA
TI Trench etch **endpoint detection** by laser-induced fluorescence
IN Bennett, Reid S.; Ephrath, Linda M.; Schwartz, Geraldine C.; Selwyn, Gary S.
PA International Business Machines Corp., USA
SO U.S., 11 pp.
PI US 4675072 A 19870623 US 1986-878144 19860625
PRAI US 1986-878144 19860625
AB Laser induced fluorescence (LIF) is utilized to detect and **control** the reactive ion **etch**-through of a given layer in a wafer by detecting a large change in the concn. of a selected minor species from the wafer in the etching plasma. As an example, CuCl generated from Cu **dopant** can be monitored in the plasma by LIF detection of its particular laser transition line. An elec. signal is indicative of the CuCl concn. in the plasma, and when the amplitude of this signal falls below a predetd. level, the given layer of the water, present in a reaction chamber, is considered to be etched through.

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